# NCV8772

# Ultra Low I$_q$ 350 mA LDO Regulator with Enable and Reset

The NCV8772 is 350 mA LDO regulator with integrated reset functions dedicated for microprocessor applications. Its robustness allows NCV8772 to be used in severe automotive environments. Ultra low quiescent current as low as 24 μA typical makes it suitable for applications permanently connected to battery requiring ultra low quiescent current with or without load. This feature is especially critical when modules remain in active mode when ignition is off. The Enable function can be used for further decrease of quiescent current in shutdown mode to 1 μA. The NCV8772 contains protection functions as current limit, thermal shutdown and reverse output current protection.

## Features

- Output Voltage Options: 3.3 V and 5 V
- Output Voltage Accuracy: ±1.5% (T$_J$ = 25°C to 125°C)
- Output Current up to 350 mA
- Ultra Low Quiescent Current: typ 24 μA (max 30 μA)
- Very Wide Range of C$_{out}$ and ESR Values for Stability
- Enable Function
  - 1 μA Max Quiescent Current when disabled
- Microprocessor Compatible Control Functions:
  - Reset with Adjustable Power−On Delay
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features
  - Current Limitation
  - Thermal Shutdown
  - Reverse Output Current Protection
- These are Pb−Free Devices

## Typical Applications

- Body Control Module
- Instruments and Clusters
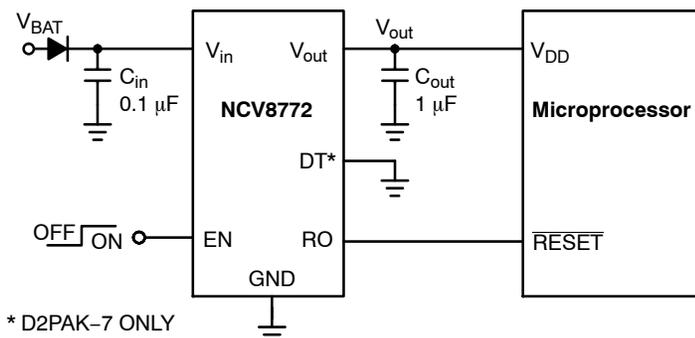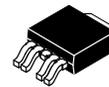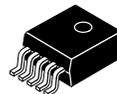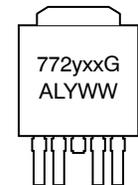- Occupant Protection and Comfort
- Powertrain

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### MARKING DIAGRAMS

DPAK−5
DT SUFFIX
CASE 175AA

772yxxG
ALYWW

D2PAK−5
D5S SUFFIX
CASE 936A

NC
V8772yxx
AWLYWWG
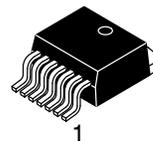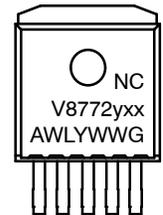
D2PAK−7
D7S SUFFIX
CASE 936AB

NC
V8772yxx
AWLYWWG
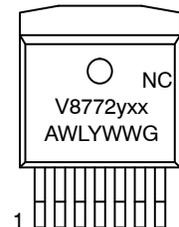
| | |
|---|---|
| y | = Timing and Reset Threshold Option |
| x, xx | = Voltage Option |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.



Figure 1. Typical Application Schematic

\* D2PAK−7 ONLY

# NCV8772
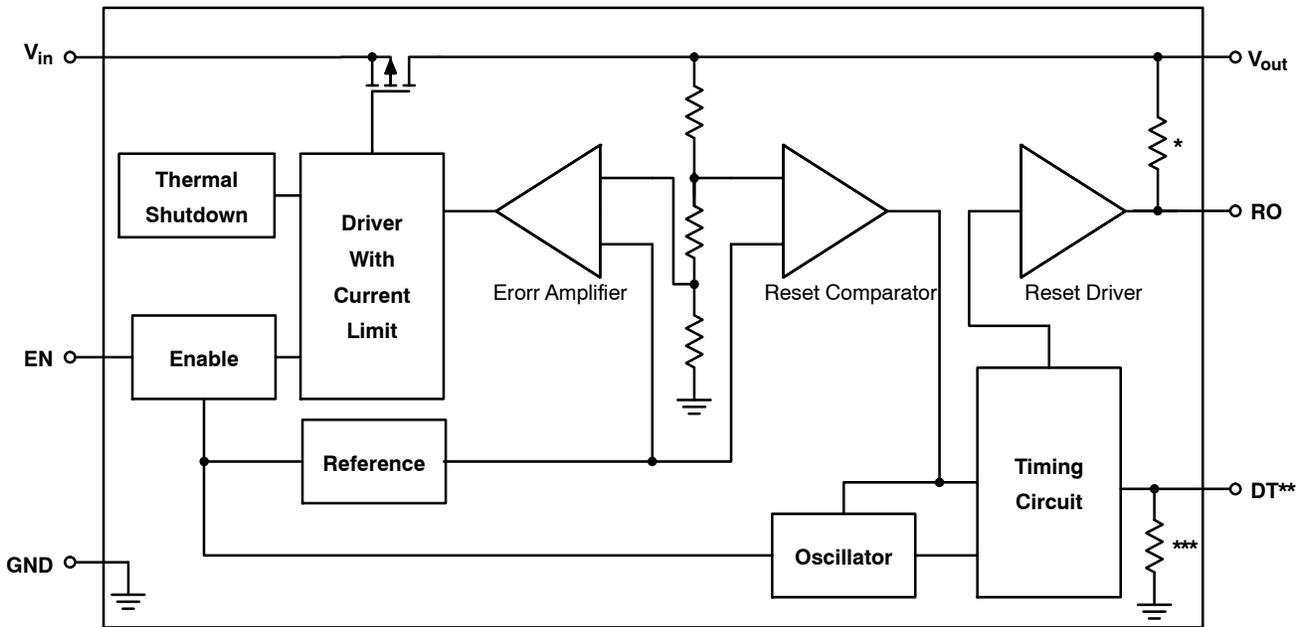


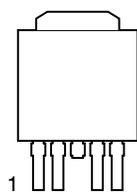* 5 V OPTION ONLY
** D2PAK−7 ONLY
*** Pull−Down Resistor (typ 150 kΩ) active only in Reset State
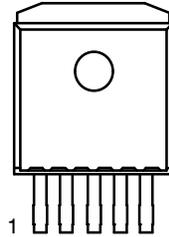
**Figure 2. Simplified Block Diagram**

## PIN CONNECTIONS

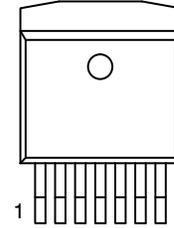

DPAK−5

PIN  1. $V_{in}$
     2. RO
Tab, 3. GND
     4. EN
     5. $V_{out}$

D$^2$PAK−5

PIN  1. $V_{in}$
     2. RO
Tab, 3. GND
     4. EN
     5. $V_{out}$

D$^2$PAK−7

PIN  1. $V_{in}$
     2. RO
     3. NC
Tab, 4. GND
     5. EN
     6. DT
     7. $V_{out}$

**Figure 3. Pin Connections**

## PIN FUNCTION DESCRIPTION

| Pin No. DPAK−5 D2PAK−5 | Pin No. D2PAK−7 | Pin Name | Description |
|---|---|---|---|
| 1 | 1 | $V_{in}$ | Positive Power Supply Input. Connect 0.1 μF capacitor to ground. |
| 2 | 2 | RO | Reset Output. 30 kΩ internal Pull−up resistor connected to $V_{out}$. RO goes Low when $V_{out}$ drops by more than 7% (typ) from its nominal value (for NCV8772y devices with y = 1,2,3,...) or more than 10% (typ) from its nominal value (for NCV8772y devices with y = A, B, C,...). |
| – | 3 | NC | Not Connected |
| 3, TAB | 4, TAB | GND | Power Supply Ground. |
| 4 | 5 | EN | Enable Input. Low level disables the IC. |
| – | 6 | DT | Reset Delay Time Select. Short to GND or connected to $V_{out}$ to select time. |
| 5 | 7 | $V_{out}$ | Regulated Output Voltage. Connect 1 μF capacitor with ESR < 100 Ω to ground. |

## ABSOLUTE MAXIMUM RATINGS

| Rating | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage (Note 1) | DC<br>Transient, t < 100 ms | $V_{in}$ | −0.3<br>− | 40<br>45 | V |
| Input Current | | $I_{in}$ | −5 | − | mA |
| Output Voltage (Note 2) | | $V_{out}$ | −0.3 | 5.5 | V |
| Output Current | | $I_{out}$ | −3 | Current Limited | mA |
| Enable Input Voltage | DC<br>Transient, t < 100 ms | $V_{EN}$ | −0.3<br>− | 40<br>45 | V |
| Enable Input Current | | $I_{EN}$ | −1 | 1 | mA |
| DT (Reset Delay Time Select) Voltage | | $V_{DT}$ | −0.3 | 5.5 | V |
| DT (Reset Delay Time Select) Current | | $I_{DT}$ | −1 | 1 | mA |
| Reset Output Voltage | | $V_{RO}$ | −0.3 | 5.5 | V |
| Reset Output Current | | $I_{RO}$ | −3 | 3 | mA |
| Junction Temperature | | $T_J$ | −40 | 150 | °C |
| Storage Temperature | | $T_{STG}$ | −55 | 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. 5.5 V or ($V_{in}$ + 0.3 V) (whichever is lower).

## ESD CAPABILITY (Note 3)

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| ESD Capability, Human Body Model | $ESD_{HBM}$ | −2 | 2 | kV |
| ESD Capability, Machine Model | $ESD_{MM}$ | −200 | 200 | V |
| ESD Capability, Charged Device Model | $ESD_{CDM}$ | −1 | 1 | kV |

3. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
    ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
    ESD Charge Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)

## LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

| Rating | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Moisture Sensitivity Level | DPAK−5<br>D2PAK−5<br>D2PAK−7 | MSL | | 1<br>1<br>3 | − |
| Lead Temperature Soldering<br>    Reflow (SMD Styles Only), Pb−Free Versions | | $T_{SLD}$ | − | 265 peak | °C |

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## THERMAL CHARACTERISTICS (Note 5)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, DPAK−5<br>    Thermal Resistance, Junction−to−Air (Note 6)<br>    Thermal Reference, Junction−to−Case (Note 6) | $R_{\theta JA}$<br>$R_{\Psi JC}$ | 56<br>8.4 | °C/W |
| Thermal Characteristics, D2PAK−5<br>    Thermal Resistance, Junction−to−Air (Note 6)<br>    Thermal Reference, Junction−to−Case (Note 6) | $R_{\theta JA}$<br>$R_{\Psi JC}$ | 53<br>8.4 | °C/W |
| Thermal Characteristics, D2PAK−7<br>    Thermal Resistance, Junction−to−Air (Note 6)<br>    Thermal Reference, Junction−to−Case (Note 6) | $R_{\theta JA}$<br>$R_{\Psi JC}$ | 51<br>8.4 | °C/W |

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
6. Values based on copper area of 645 mm$^2$ (or 1 in$^2$) of 1 oz copper thickness and FR4 PCB substrate.

## RECOMMENDED OPERATING RANGE (Note 7)

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage (Note 8) | $V_{in}$ | 4.5 | 40 | V |
| Junction Temperature | $T_J$ | −40 | 150 | °C |

7. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
8. Minimum $V_{in}$ = 4.5 V or ($V_{out}$ + $V_{DO}$), whichever is higher.

**ELECTRICAL CHARACTERISTICS** $V_{in}$ = 13.2 V, $V_{EN}$ = 3 V, $C_{in}$ = 0.1 μF, $C_{out}$ = 1 μF, for typical values $T_J$ = 25°C, for min/max values $T_J$ = −40°C to 150°C; unless otherwise noted. (Notes 9 and 10)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **REGULATOR OUTPUT** | | | | | | |
| Output Voltage (Accuracy %)<br>3.3 V<br>5.0 V | $T_J$ = 25 °C to 125 °C<br>$V_{in}$ = 4.5 V to 16 V, $I_{out}$ = 0.1 mA to 200 mA<br>$V_{in}$ = 5.575 V to 16 V, $I_{out}$ = 0.1 mA to 200 mA | $V_{out}$ | 3.2505<br>4.925<br>(−1.5 %) | 3.3<br>5.0 | 3.3495<br>5.075<br>(+1.5%) | V |
| Output Voltage (Accuracy %)<br>3.3 V<br><br>5.0 V | $V_{in}$ = 4.5 V to 40 V, $I_{out}$ = 0.1 mA to 200 mA<br>$V_{in}$ = 4.5 V to 16 V, $I_{out}$ = 0.1 mA to 350 mA<br>$V_{in}$ = 5.6 V to 40 V, $I_{out}$ = 0.1 mA to 200 mA<br>$V_{in}$ = 5.975 V to 16 V, $I_{out}$ = 0.1 mA to 350 mA | $V_{out}$ | 3.234<br>3.234<br>4.9<br>4.9<br>(−2 %) | 3.3<br>3.3<br>5.0<br>5.0 | 3.366<br>3.366<br>5.1<br>5.1<br>(+2%) | V |
| Output Voltage (Accuracy %)<br>3.3 V<br>5.0 V | $T_J$ = −40°C to 125°C<br>$V_{in}$ = 4.5 V to 28 V, $I_{out}$ = 0 mA to 350 mA<br>$V_{in}$ = 5.975 V to 28 V, $I_{out}$ = 0 mA to 350 mA | $V_{out}$ | 3.234<br>4.9<br>(−2 %) | 3.3<br>5.0 | 3.366<br>5.1<br>(+2%) | V |
| Line Regulation<br>3.3 V<br>5.0 V | $V_{in}$ = 4.5 V to 28 V, $I_{out}$ = 5 mA<br>$V_{in}$ = 6 V to 28 V, $I_{out}$ = 5 mA | $Reg_{line}$ | −20 | 0 | 20 | mV |
| Load Regulation | $I_{out}$ = 0.1 mA to 350 mA | $Reg_{load}$ | −35 | 10 | 35 | mV |
| Dropout Voltage (Note 11)<br>5.0 V | $I_{out}$ = 200 mA<br>$I_{out}$ = 350 mA | $V_{DO}$ | –<br>– | 250<br>440 | 500<br>875 | mV |
| Output Capacitor for Stability (Note 12) | $I_{out}$ = 0 mA to 350 mA | $C_{out}$<br>ESR | 1<br>0.01 | –<br>– | 100<br>100 | μF<br>Ω |
| **DISABLE AND QUIESCENT CURRENTS** | | | | | | |
| Disable Current | $V_{EN}$ = 0 V, $T_J$ < 85°C | $I_{DIS}$ | – | – | 1 | μA |
| Quiescent Current ($I_q$ = $I_{in}$ − $I_{out}$) | $I_{out}$ = 0.1 mA, $T_J$ = 25°C<br>$I_{out}$ = 0.1 mA to 350 mA, $T_J$ ≤ 125°C | $I_q$ | –<br>– | 24<br>– | 29<br>30 | μA |
| **CURRENT LIMIT PROTECTION** | | | | | | |
| Current Limit | $V_{out}$ = 0.96 x $V_{out\_nom}$ | $I_{LIM}$ | 400 | – | 1100 | mA |
| Short Circuit Current Limit | $V_{out}$ = 0 V | $I_{SC}$ | 400 | – | 1100 | mA |
| **REVERSE OUTPUT CURRENT PROTECTION** | | | | | | |
| Reverse Output Current Protection | $V_{EN}$ = 0 V, $I_{out}$ = −1 mA | $V_{out\_rev}$ | – | 2 | 5.5 | V |
| **PSRR** | | | | | | |
| Power Supply Ripple Rejection (Note 12) | f = 100 Hz, 0.5 $V_{pp}$ | PSRR | – | 60 | – | dB |

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A$ ≈ $T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Measured when output voltage falls 100 mV below the regulated voltage at $V_{in}$ = 13.2 V.
12. Values based on design and/or characterization.
13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options

**ELECTRICAL CHARACTERISTICS** $V_{in}$ = 13.2 V, $V_{EN}$ = 3 V, $C_{in}$ = 0.1 μF, $C_{out}$ = 1 μF, for typical values $T_J$ = 25°C, for min/max values $T_J$ = −40°C to 150°C; unless otherwise noted. (Notes 9 and 10)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **ENABLE THRESHOLDS** | | | | | | |
| Enable Input Threshold Voltage<br>    Logic Low<br>    Logic High | | $V_{th(EN)}$ | –<br>2.5 | –<br>– | 0.8<br>– | V |
| Enable Input Current<br>    Logic High<br>    Logic Low | $V_{EN}$ = 5 V<br>$V_{EN}$ = 0 V, $T_J$ < 85°C | $I_{EN\_ON}$<br>$I_{EN\_OFF}$ | –<br>– | 3<br>0.5 | 5<br>1 | μA |
| **DT (RESET DELAY TIME SELECT) – D2PAK–7 ONLY** | | | | | | |
| DT Threshold Voltage<br>    Logic Low<br>    Logic High | | $V_{th(DT)}$ | –<br>2.0 | –<br>– | 0.8<br>– | V |
| DT Input Current | $V_{DT}$ = 5 V | $I_{DT}$ | – | – | 1.0 | μA |
| **RESET OUTPUT RO** | | | | | | |
| Input Voltage Reset Threshold                 3.3 V | $V_{in}$ decreasing, $V_{out} > V_{RT}$ | $V_{in\_RT}$ | – | 3.8 | 4.2 | V |
| Output Voltage Reset Threshold<br>(Note 13)<br>(NCV8772y) where y = 1,2,3,...    3.3 V<br>                                           5.0 V<br>(NCV8772y) where y = A,B,C,...    3.3 V<br>                                           5.0 V | $V_{out}$ decreasing<br><br>$V_{in} > 4.5$ V<br>$V_{in} > 5.5$ V<br>$V_{in} > 4.5$ V<br>$V_{in} > 5.5$ V | $V_{RT}$ | <br><br>90<br>90<br>87<br>87 | <br><br>93<br>93<br>90<br>90 | <br><br>96<br>96<br>93<br>93 | %$V_{out}$ |
| Reset Hysteresis | | $V_{RH}$ | – | 2.0 | – | %$V_{out}$ |
| Maximum Reset Sink Current          3.3 V<br>                                           5.0 V | $V_{out}$ = 3 V, $V_{RO}$ = 0.25 V<br>$V_{out}$ = 4.5 V, $V_{RO}$ = 0.25 V | $I_{ROmax}$ | 1.3<br>1.75 | –<br>– | –<br>– | mA |
| Reset Output Low Voltage | $V_{out} > 1$ V, $I_{RO} < 200$ μA | $V_{ROL}$ | – | 0.15 | 0.25 | V |
| Reset Output High Voltage          5.0 V | | $V_{ROH}$ | 4.5 | – | – | V |
| Reset High Level Leakage Current<br>                                           3.3 V | | $I_{ROLK}$ | – | – | 1.0 | μA |
| Integrated Reset Pull–up Resistor<br>                                           5.0 V | | $R_{RO}$ | 15 | 30 | 50 | kΩ |
| Reset Delay Time (DPAK–5, D2PAK–5)<br>(Note 13) | Min Available Time<br>Max Available Time | $t_{RD}$ | 6.4<br>102.4<br>(20%) | 8.0<br>128 | 9.6<br>153.6<br>(20%) | ms |
| Reset Delay Time (D2PAK–7)<br>(Note 13) | Min Available Time, DT connected to GND<br>Max Available Time, DT connected to $V_{out}$ | $t_{RD}$ | 3.2<br>102.4<br>(20%) | 4.0<br>128 | 4.8<br>153.6<br>(20%) | ms |
| Reset Reaction Time (see Figure 33) | | $t_{RR}$ | 16 | 25 | 38 | μs |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown Temperature<br>(Note 12) | | $T_{SD}$ | 150 | 175 | 195 | °C |
| Thermal Shutdown Hysteresis<br>(Note 12) | | $T_{SH}$ | – | 25 | – | °C |

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Measured when output voltage falls 100 mV below the regulated voltage at $V_{in}$ = 13.2 V.
12. Values based on design and/or characterization.
13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options

# NCV8772

## TYPICAL CHARACTERISTICS



$V_{in}$ = 13.2 V
$I_{out}$ = 100 μA
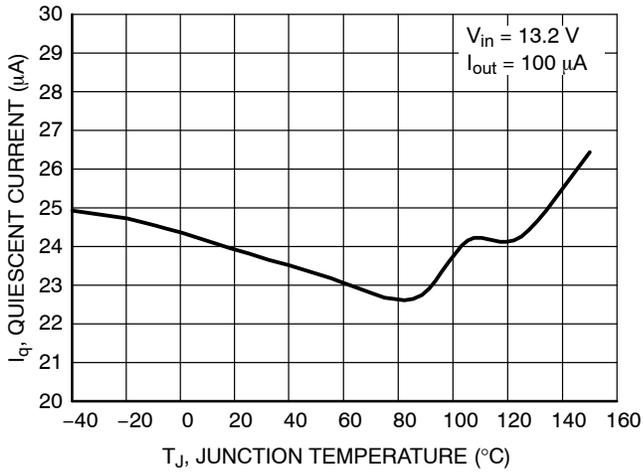
**Figure 4. Quiescent Current vs. Temperature**



$I_{out}$ = 0 mA
$T_J$ = 25°C
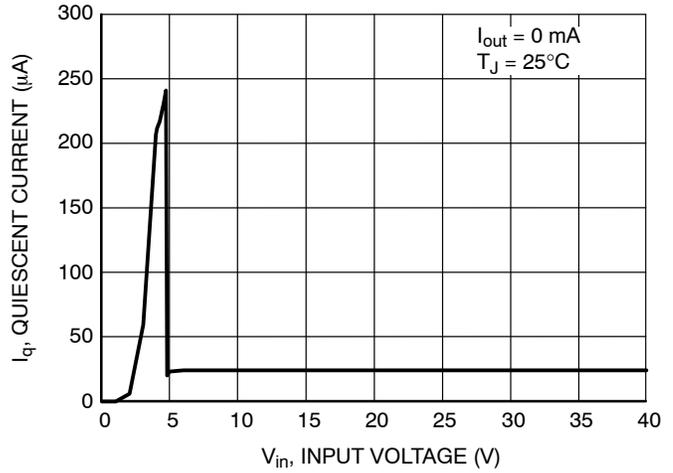
**Figure 5. Quiescent Current vs. Input Voltage**



$V_{in}$ = 13.2 V

$T_J$ = 150°C

$T_J$ = −40°C

$T_J$ = 25°C
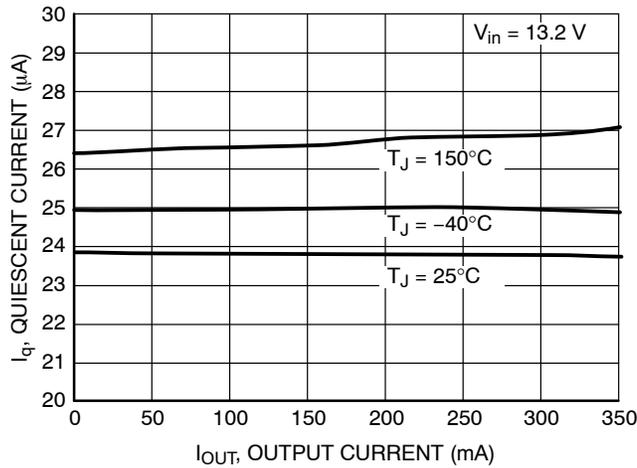
**Figure 6. Quiescent Current vs. Output Current**



$V_{in}$ = 13.2 V
$I_{out}$ = 100 μA
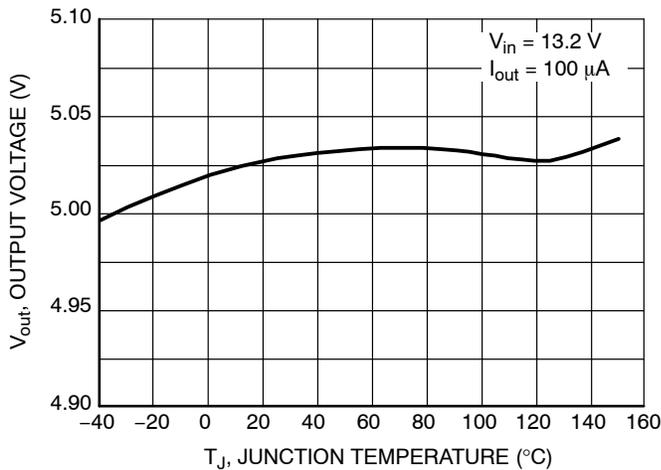
**Figure 7. Output Voltage vs. Temperature
(5 V Option)**



$V_{in}$ = 13.2 V
$I_{out}$ = 100 μA
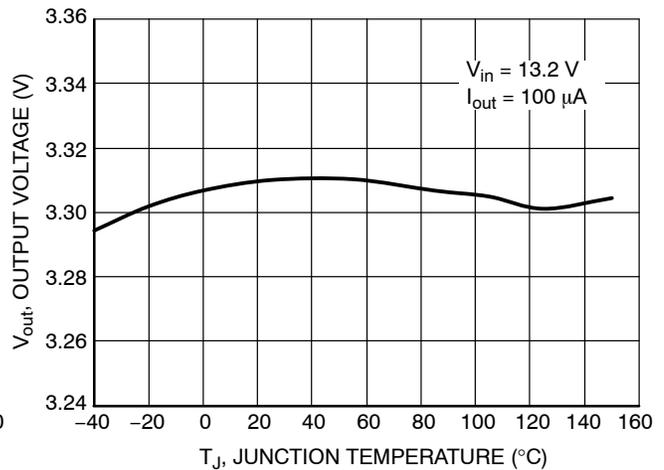
**Figure 8. Output Voltage vs. Temperature
(3.3 V Option)**

## TYPICAL CHARACTERISTICS
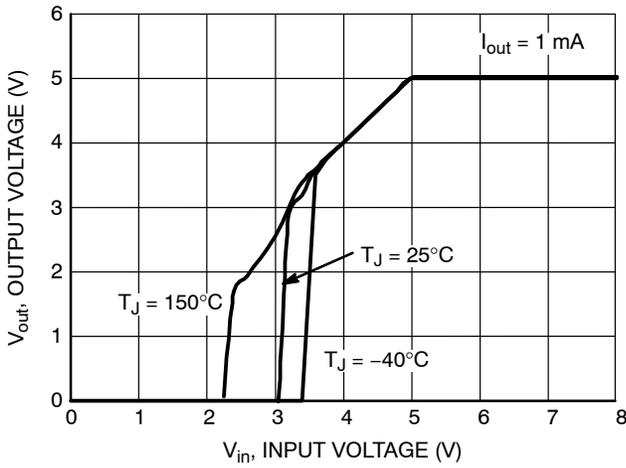


**Figure 9. Output Voltage vs. Input Voltage
(5 V Option)**
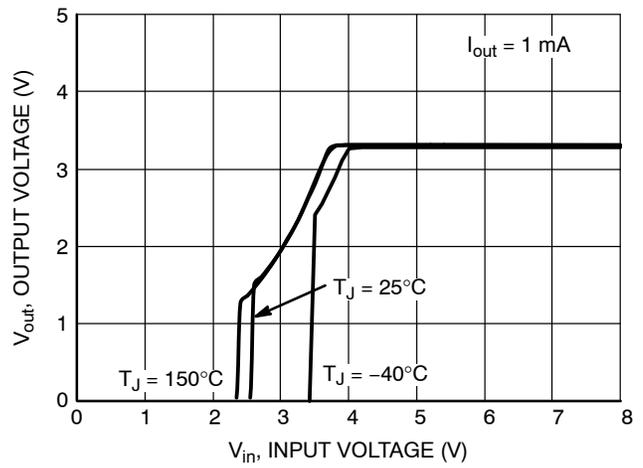


**Figure 10. Output Voltage vs. Input Voltage
(3.3 V Option)**
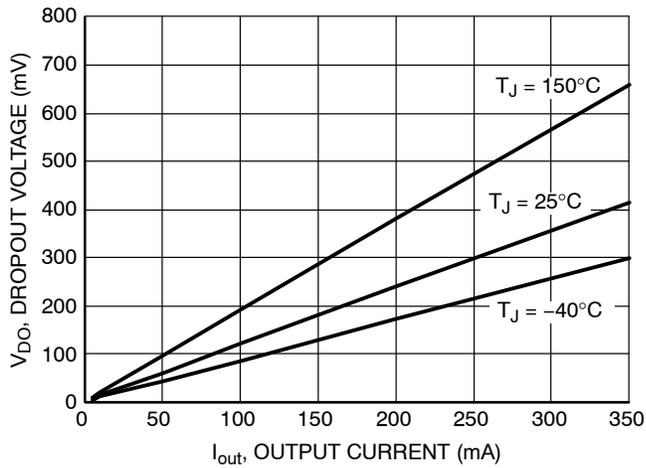


**Figure 11. Dropout vs. Output Current
(5 V Option)**
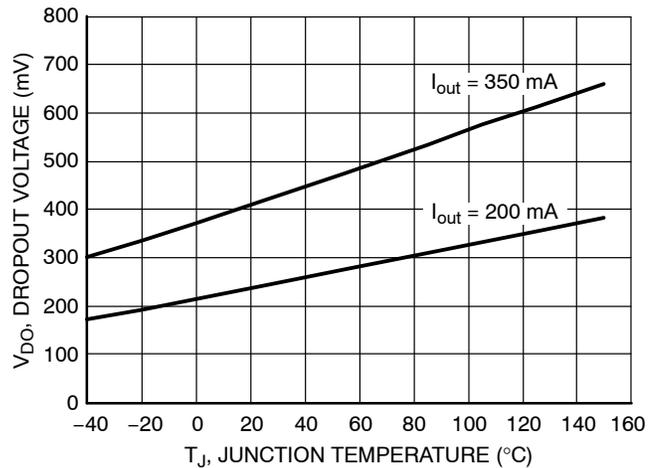


**Figure 12. Dropout vs. Temperature
(5 V Option)**

## TYPICAL CHARACTERISTICS
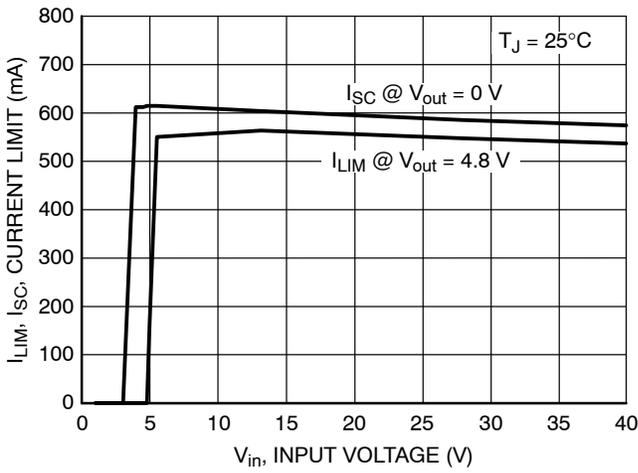


**Figure 13. Output Current Limit vs. Input Voltage (5 V Option)**
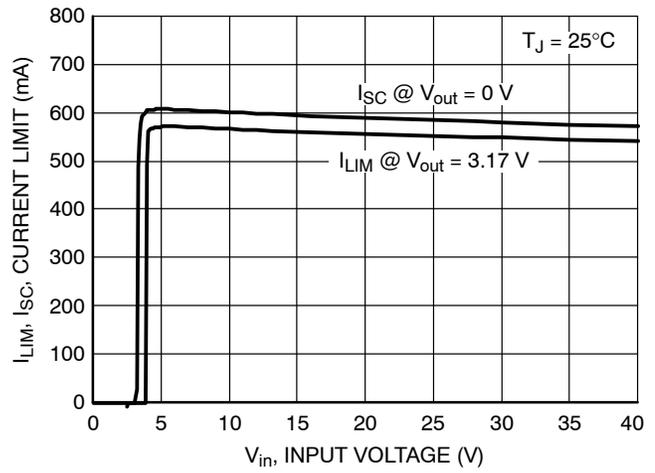


**Figure 14. Output Current Limit vs. Input Voltage (3.3 V Option)**
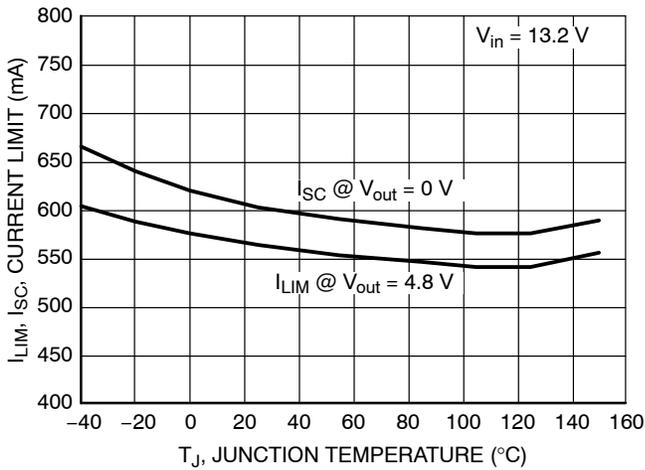


**Figure 15. Output Current Limit vs. Temperature (5 V Option)**
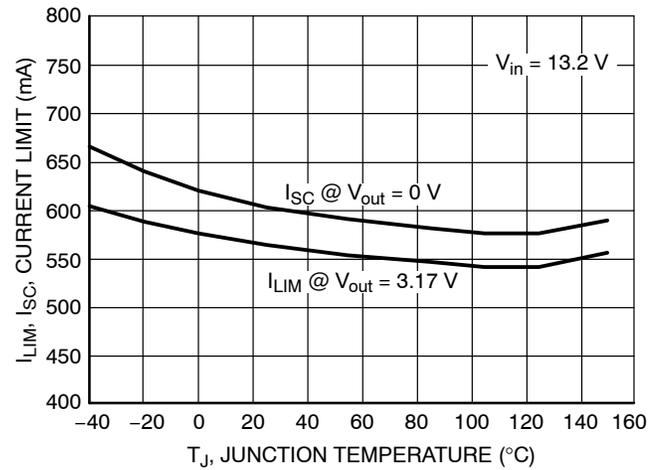


**Figure 16. Output Current Limit vs. Temperature (3.3 V Option)**
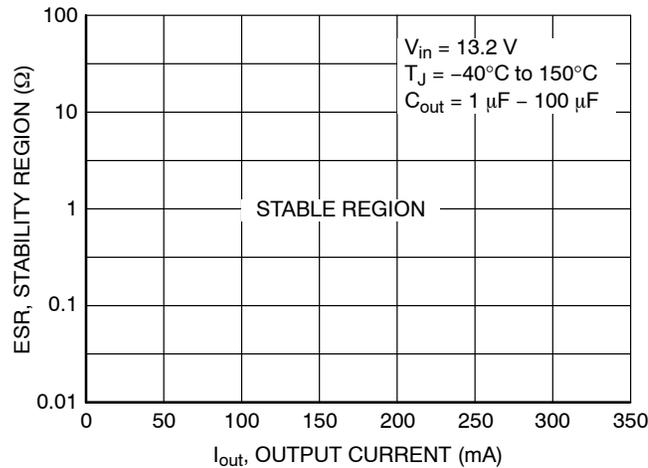


**Figure 17. $C_{out}$ ESR Stability Region vs. Output Current**

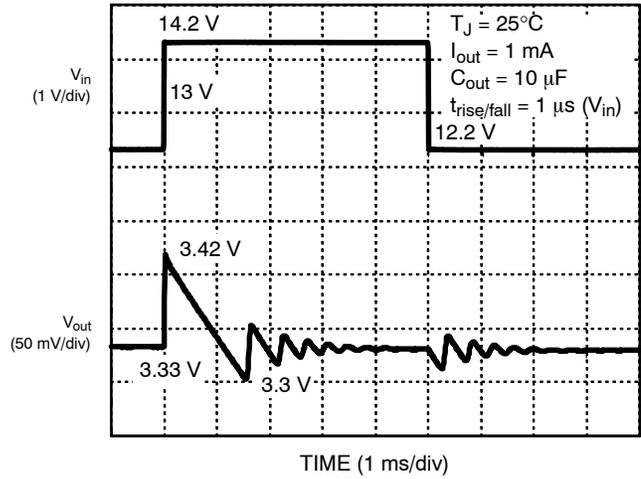## TYPICAL CHARACTERISTICS
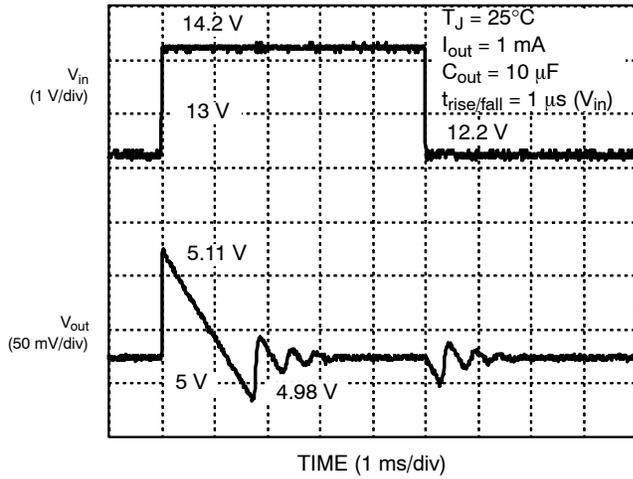


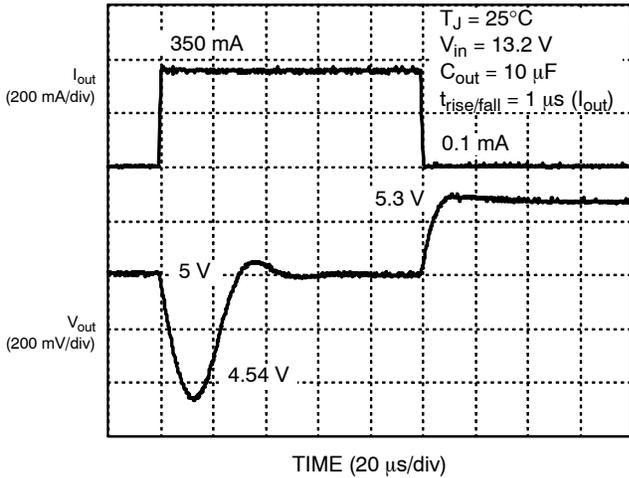**Figure 18. Line Transients
(5 V Option)**



**Figure 19. Line Transients
(3.3 V Option)**
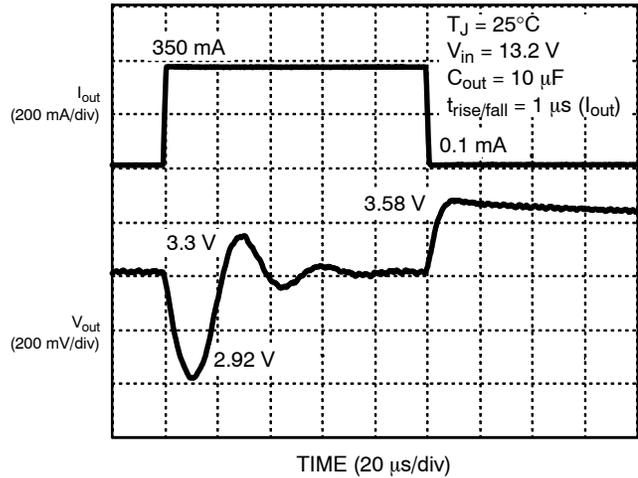


**Figure 20. Load Transients
(5 V Option)**



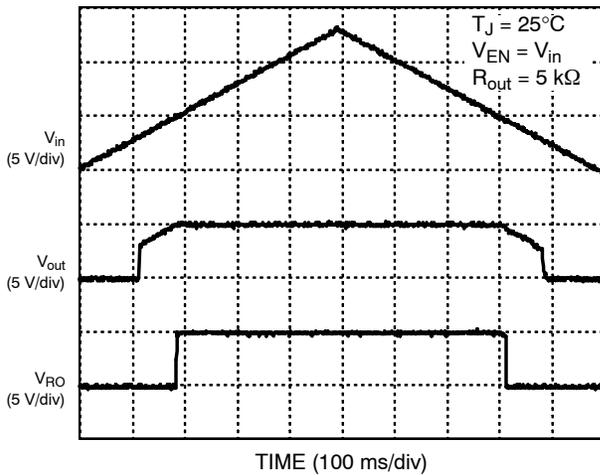**Figure 21. Load Transients
(3.3 V Option)**
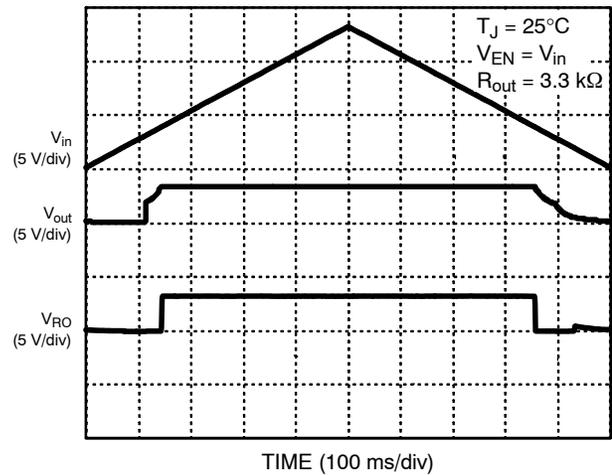


**Figure 22. Power Up/Down Response
(5 V Option)**



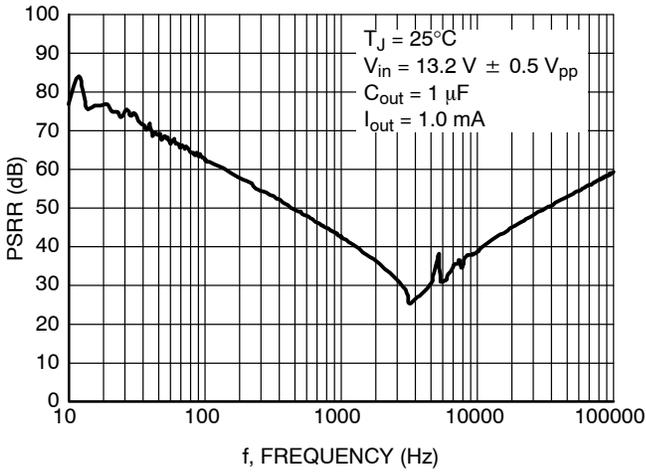**Figure 23. Power Up/Down Response
(3.3 V Option)**

## TYPICAL CHARACTERISTICS
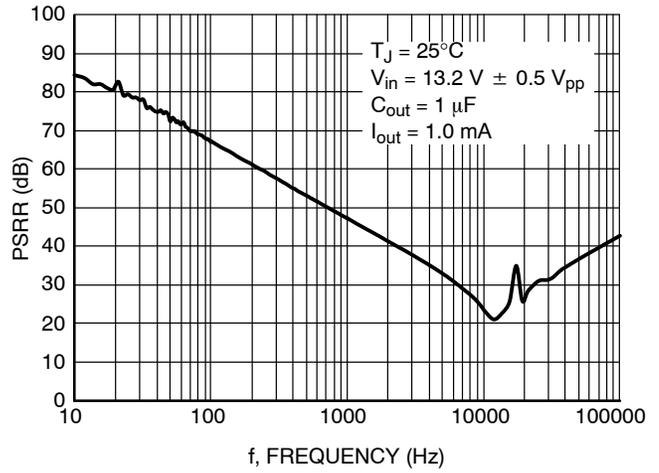


**Figure 24. PSRR vs. Frequency (5 V Option)**

$T_J = 25°C$
$V_{in} = 13.2\ V \pm 0.5\ V_{pp}$
$C_{out} = 1\ \mu F$
$I_{out} = 1.0\ mA$



**Figure 25. PSRR vs. Frequency (3.3 V Option)**

$T_J = 25°C$
$V_{in} = 13.2\ V \pm 0.5\ V_{pp}$
$C_{out} = 1\ \mu F$
$I_{out} = 1.0\ mA$
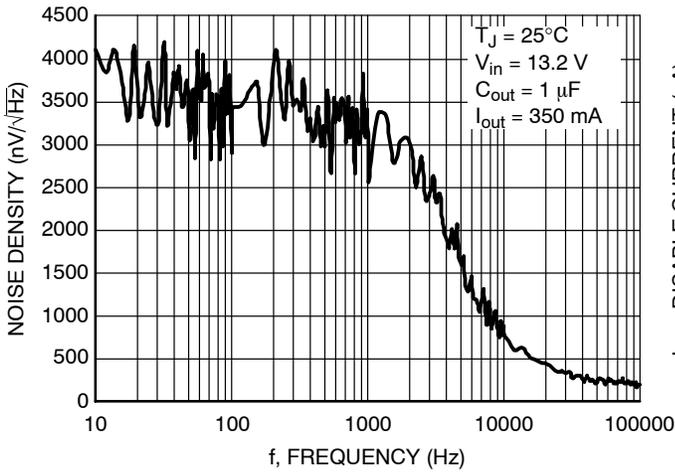


**Figure 26. Noise vs. Frequency**

$T_J = 25°C$
$V_{in} = 13.2\ V$
$C_{out} = 1\ \mu F$
$I_{out} = 350\ mA$
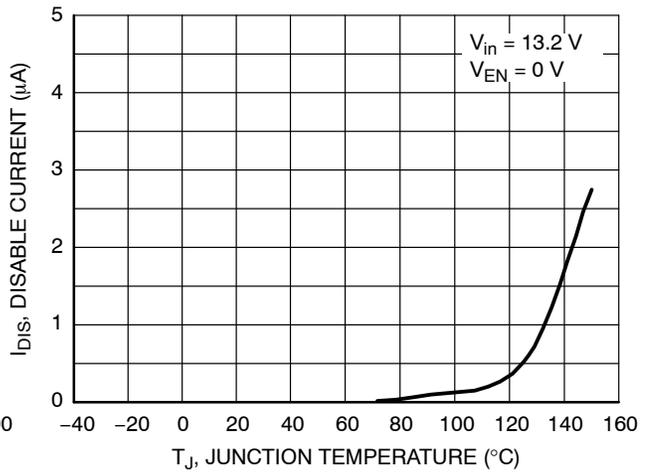


**Figure 27. Disable Current vs. Temperature**

$V_{in} = 13.2\ V$
$V_{EN} = 0\ V$
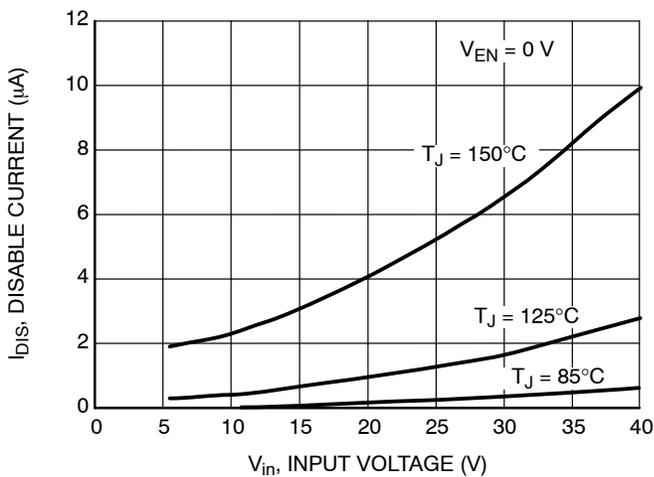


**Figure 28. Disable Current vs. Input Voltage**

$V_{EN} = 0\ V$
$T_J = 150°C$
$T_J = 125°C$
$T_J = 85°C$
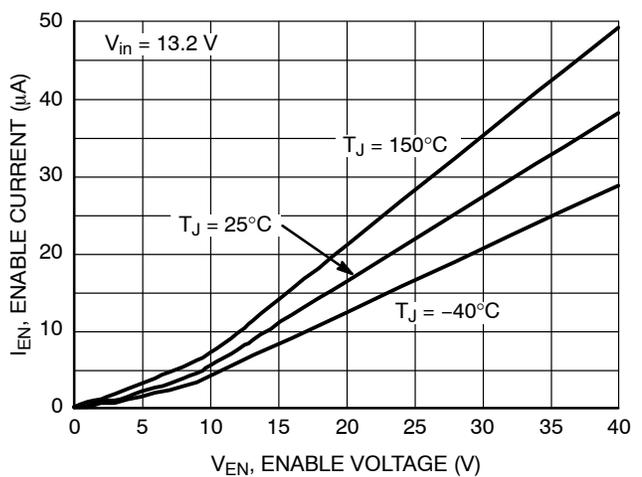


**Figure 29. Enable Current vs. Enable Voltage**

$V_{in} = 13.2\ V$
$T_J = 150°C$
$T_J = 25°C$
$T_J = -40°C$
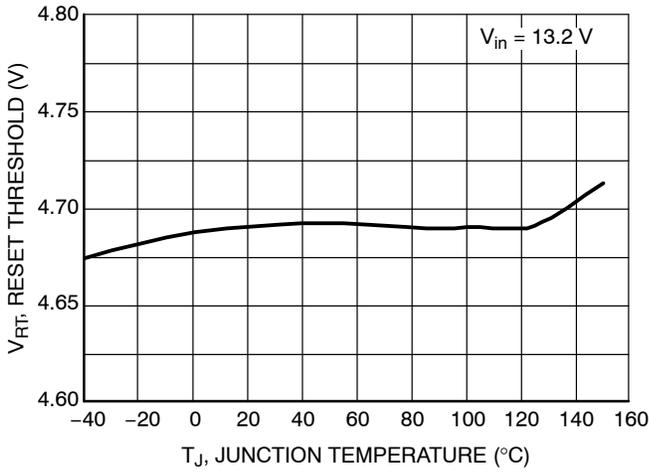
## TYPICAL CHARACTERISTICS



**Figure 30. Reset Threshold vs. Temperature (5 V Option)**
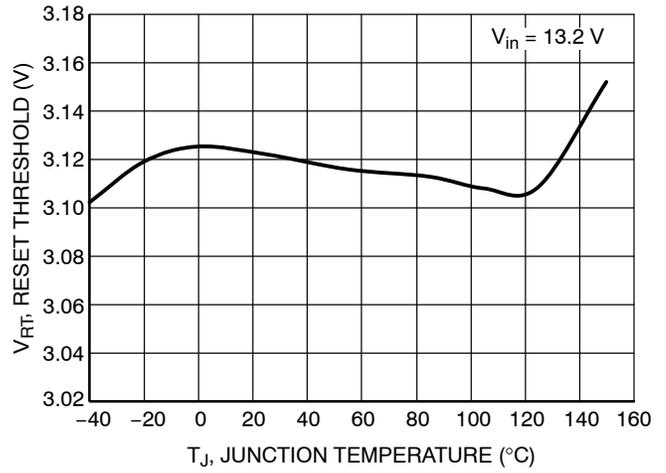


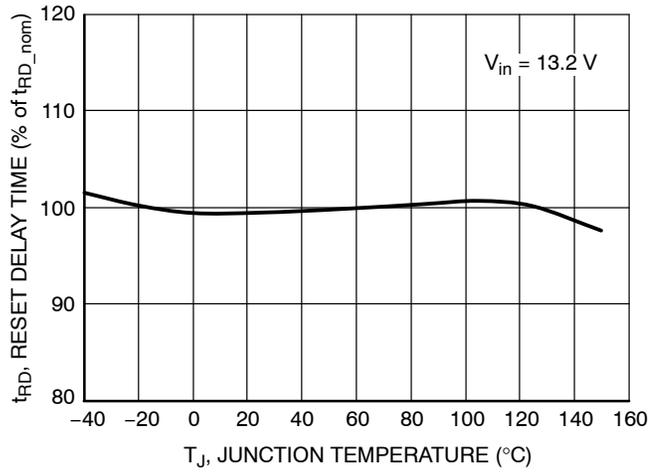**Figure 31. Reset Threshold vs. Temperature (3.3 V Option)**



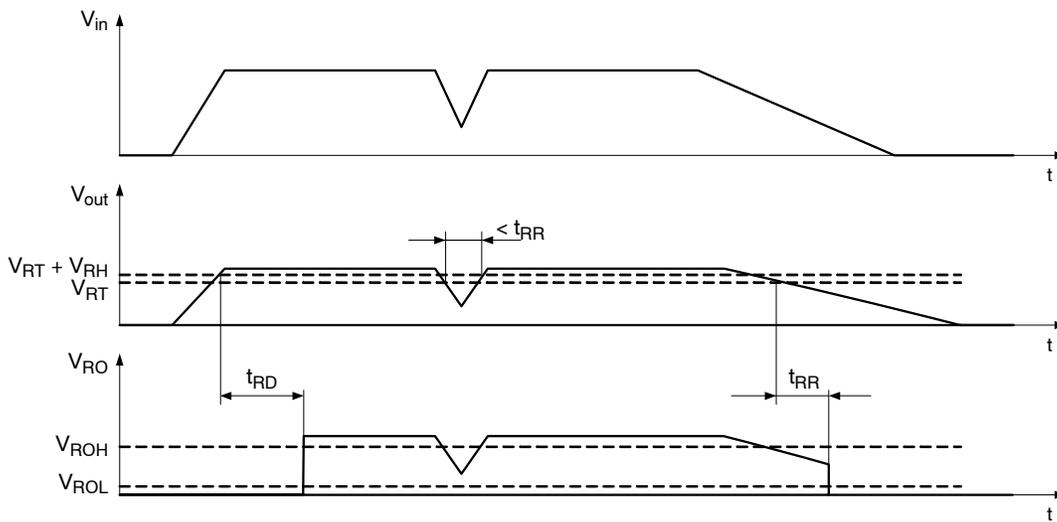**Figure 32. Reset Delay Time vs. Temperature**



**Figure 33. Reset Function and Timing Diagram**

# NCV8772

## DEFINITIONS

### General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

### Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

### Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

### Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

### Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

### Quiescent and Disable Currents

Quiescent Current ($I_q$) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current ($I_{DIS}$).

### Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

### PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

### Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

### Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

### Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

### Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

## APPLICATIONS INFORMATION

The NCV8772 regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figure 4 to Figure 33.

### Input Decoupling (C$_{in}$)

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8772 package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

### Output Decoupling (C$_{out}$)

The NCV8772 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs Output Current is shown in Figure 17. The minimum output decoupling value is 1 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

### Enable Operation

The Enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this datasheet.

### Reset Operation

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 33. This is in the form of a logic signal on RO. Output voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to V$_{out}$ = 1.0 V. For 5 V voltage option, the Reset Output (RO) circuitry includes internal pull−up (30 kΩ) connected to the output (V$_{out}$) No external pull−up is necessary.

### RESET DELAY AND RESET THRESHOLD OPTIONS (DPAK−5 AND D2PAK−5)

|  | Reset Delay Time | Reset Threshold |
|---|---|---|
| NCV87721DT<br>NCV87721D5S | 8 ms | 93% |
| NCV87722DT<br>NCV87722D5S | 16 ms | 93% |
| NCV87723DT<br>NCV87723D5S | 32 ms | 93% |
| NCV87724DT<br>NCV87724D5S | 64 ms | 93% |
| NCV87725DT<br>NCV87725D5S | 128 ms | 93% |
| NCV8772ADT<br>NCV8772AD5S | 8 ms | 90% |
| NCV8772BDT<br>NCV8772BD5S | 16 ms | 90% |
| NCV8772CDT<br>NCV8772CD5S | 32 ms | 90% |
| NCV8772DDT<br>NCV8772DD5S | 64 ms | 90% |
| NCV8772EDT<br>NCV8772ED5S | 128 ms | 90% |

NOTE: The timing values can be selected from the following list: 8, 16, 32, 64, 128 ms. Contact factory for options not included in ORDERING INFORMATION table on page 14.

### Reset Delay Time Select (D2PAK−7 only)

Selection of the NCV8772yD7S devices and the state of the DT pin determines the available Reset Delay times. The part is designed for use with DT tied to ground or V$_{out}$, but may be controlled by any logic signal which provides a threshold between 0.8 V and 2 V. The default condition for an open DT pin is the slower Reset time (DT = GND condition). Times are in pairs and are highlighted in the chart below. Consult factory for availability. The Delay Time select (DT) pin is logic level controlled and provides Reset Delay time per the chart. Note the DT pin is sampled only when RO is low, and changes to the DT pin when RO is high will not effect the reset delay time.

**RESET DELAY AND RESET THRESHOLD OPTIONS (D2PAK−7)**

| | DT = GND Reset Time | DT = V_out Reset Time | Reset Threshold |
|---|---|---|---|
| NCV87721D7S | 8 ms | 128 ms | 93% |
| NCV87722D7S | 8 ms | 32 ms | 93% |
| NCV87723D7S | 16 ms | 64 ms | 93% |
| NCV87724D7S | 32 ms | 128 ms | 93% |
| NCV87725D7S | 4 ms | 8 ms | 93% |
| NCV8772AD7S | 8 ms | 128 ms | 90% |
| NCV8772BD7S | 8 ms | 32 ms | 90% |
| NCV8772CD7S | 16 ms | 64 ms | 90% |
| NCV8772DD7S | 32 ms | 128 ms | 90% |
| NCV8772ED7S | 4 ms | 8 ms | 90% |

NOTE:    The timing values can be selected from the following list: 4, 8, 16, 32, 64, 128 ms. Contact factory for options not included in ORDERING INFORMATION table on page 14.

**Thermal Considerations**

As power in the NCV8772 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8772 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8772 can handle is given by:

$$P_{D(max)} = \frac{\left[ T_{J(max)} - T_A \right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since $T_J$ is not recommended to exceed 150°C, then the NCV8772 soldered on 645 mm$^2$, 1 oz copper area, FR4 can

dissipate up to 2.35 W (for D2PAK−5) when the ambient temperature ($T_A$) is 25°C. See Figure 34 for $R_{\theta JA}$ versus PCB area. The power dissipated by the NCV8772 can be calculated from the following equations:

$$P_D = V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 2)}$$

or

$$V_{in(max)} = \frac{P_{D(max)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 3)}$$

NOTE:    Items containing $I_q$ can be neglected if $I_{out} \gg I_q$.



**Figure 34. Thermal Resistance vs. PCB Copper Area (D2PAK−5)**

**Hints**

$V_{in}$ and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8772 and make traces as short as possible.

**ORDERING INFORMATION**

| Device | Output Voltage | Reset Delay Time (DT = GND/V_out for D2PAK−7) | Reset Threshold | Marking | Package | Shipping† |
|---|---|---|---|---|---|---|
| NCV87722DT50RKG | 5.0 V | 16 ms | 93% | 772250G | DPAK−5 (Pb−Free) | 2500 / Tape & Reel |
| NCV87721D5S50R4G | 5.0 V | 8 ms | 93% | NC V8772150 | D2PAK−5 (Pb−Free) | 800 / Tape & Reel |
| NCV87725D7S50R4G | 5.0 V | 4/8 ms | 93% | NC V8772550 | D2PAK−7 (Pb−Free) | 750 / Tape & Reel |
| NCV87722DT33RKG | 3.3 V | 16 ms | 93% | 772233G | DPAK−5 (Pb−Free) | 2500 / Tape & Reel |
| NCV87722D5S33R4G | 3.3 V | 16 ms | 93% | NC V8772233 | D2PAK−5 (Pb−Free) | 800 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
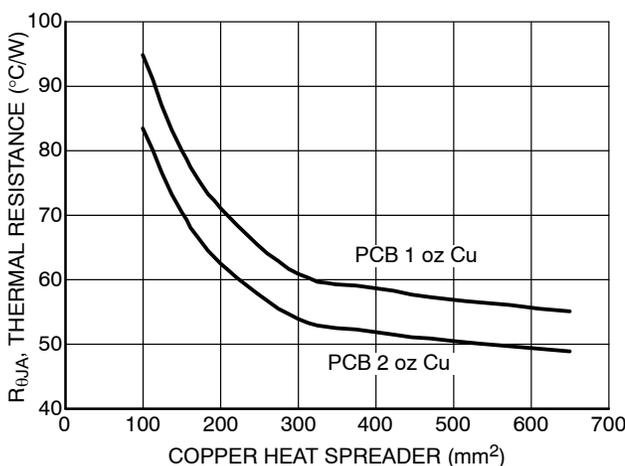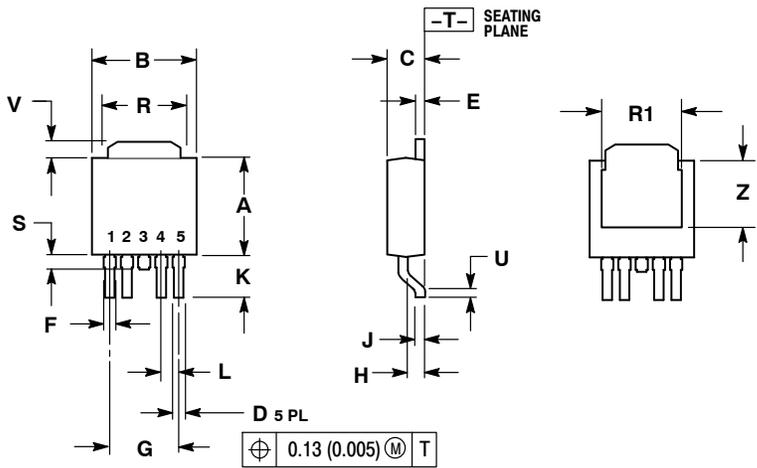
# NCV8772
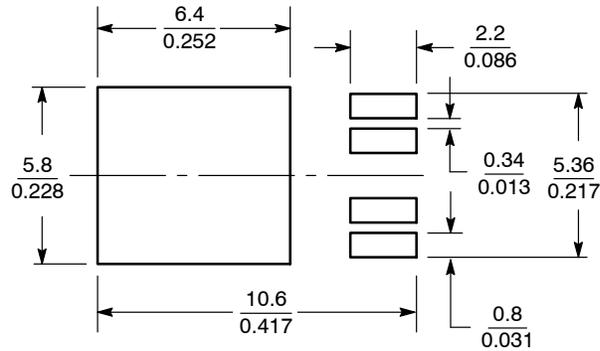
## PACKAGE DIMENSIONS

**DPAK 5, CENTER LEAD CROP**
CASE 175AA
ISSUE A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

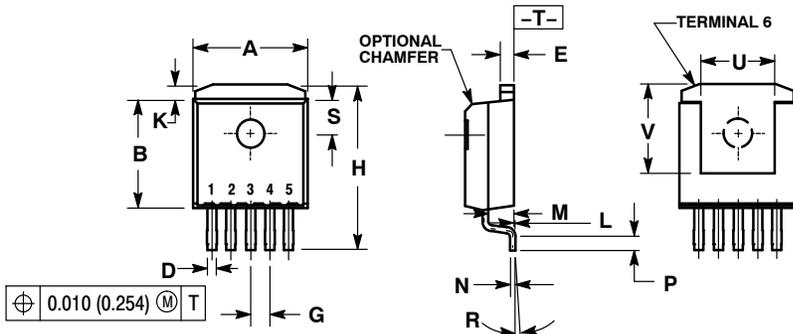| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-----|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.020 | 0.028 | 0.51 | 0.71 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.024 | 0.032 | 0.61 | 0.81 |
| G | 0.180 BSC | | 4.56 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.045 BSC | | 1.14 BSC | |
| R | 0.170 | 0.190 | 4.32 | 4.83 |
| R1 | 0.185 | 0.210 | 4.70 | 5.33 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | --- | 0.51 | --- |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | 0.170 | 3.93 | 4.32 |

## SOLDERING FOOTPRINT*

SCALE 4:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCV8772

## PACKAGE DIMENSIONS

**D²PAK 5**
CASE 936A–02
ISSUE C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|-------------|--------|
|     | MIN | MAX | MIN | MAX |
| A | 0.386 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| E | 0.045 | 0.055 | 1.143 | 1.397 |
| G | 0.067 BSC | | 1.702 BSC | |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| K | 0.050 REF | | 1.270 REF | |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | 5° REF | | 5° REF | |
| S | 0.116 REF | | 2.946 REF | |
| U | 0.200 MIN | | 5.080 MIN | |
| V | 0.250 MIN | | 6.350 MIN | |

**SOLDERING FOOTPRINT\***
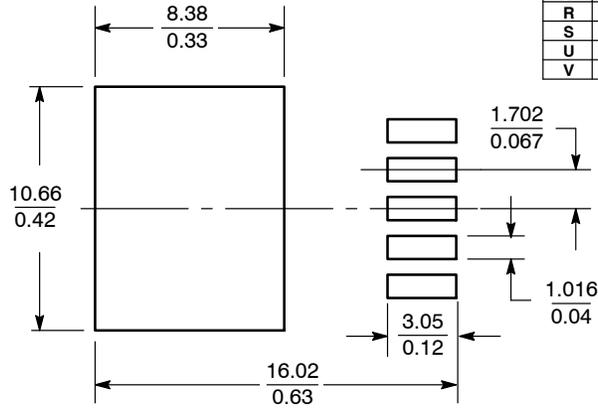
SCALE 3:1 $\left(\frac{mm}{inches}\right)$

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCV8772

## PACKAGE DIMENSIONS

### D²PAK–7 (SHORT LEAD)
CASE 936AB–01
ISSUE B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.  MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.386 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| E | 0.045 | 0.055 | 1.143 | 1.397 |
| G | 0.067 BSC | | 1.702 BSC | |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| K | 0.050 REF | | 1.270 REF | |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | 5° REF | | 5° REF | |
| S | 0.116 REF | | 2.946 REF | |
| U | 0.200 MIN | | 5.080 MIN | |
| V | 0.250 MIN | | 6.350 MIN | |

### RECOMMENDED SOLDERING FOOTPRINT*

0.424
0.310
0.584
0.136
7X 0.040
0.050 PITCH
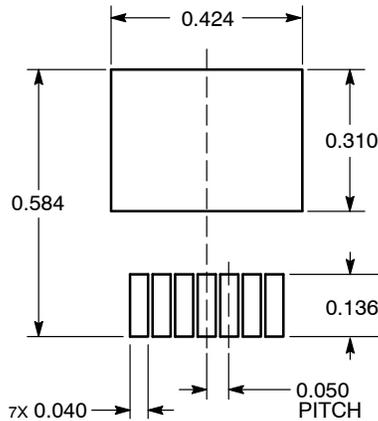
DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**NCV8772/D**